REMARKS

This is a response to the Office Action dated April 7, 2003. Claims 1-23 are pending in the present application. Reconsideration and allowance of pending claims 1-23 in view of the following remarks are requested.

A. Objection to Cross Hatching Patterns in the Drawings

Applicant acknowledges the Examiner's objection to the cross hatching patterns in the drawings. However, Applicant respectfully requests that corrections to the drawings be postponed until the time of allowance of the present application.

B. Claim Rejections

The Examiner has rejected claims 1-23 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,640,048 to Erich Selna ("Selna") in view of U.S. patent number 5,942,797 to Noriho Terasawa ("Terasawa"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 1 and 14, is patentably distinguishable over Selna and Terasawa, singly or in combination.

The present invention, as defined by independent claim 1, teaches, among other things, first and second semiconductor dies attached to a top surface of a substrate and first and second heat spreaders attached to a bottom surface of the substrate, where the first and second semiconductor dies are connected to the first and second heat spreaders by first and second vias, respectively. As disclosed in the present application, by connecting two semiconductor dies that are attached to the top surface of a substrate to

respective heat spreaders that are attached to the bottom surface of the substrate, the present invention achieves a two-die leadless carrier that provides effective thermal conduction of excess heat away from the dies by way of respective support pads, vias, and heat spreaders while comprising a single substrate. Furthermore, the present invention also provides a low resistance, low inductance, minimal length electrical ground connection between the semiconductor dies and heat spreaders by way of respective vias, which couple the semiconductor dies to the heat spreaders.

In contrast to the present invention as defined by independent claim 1, Selna does not teach, disclose, or suggest first and second semiconductor dies attached to a top surface of a substrate and first and second heat spreaders attached to a bottom surface of the substrate, where the first and second semiconductor dies are connected to the first and second heat spreaders by first and second vias, respectively. Selna specifically discloses BGA package 50, which includes IC die 12 attached to the upper surface of BGA package 50 and trace 10C attached to the lower surface of BGA package 50. See, for example, column 7, lines 5-12 and Figure 2 of Selna. However, Selna does not teach, disclose, or suggest attaching two semiconductor dies to a top surface of a substrate and connecting the two dies to heat spreaders attached to the bottom surface of the substrate by vias, respectively.

In contrast to the present invention as defined by independent claim 1, Terasawa does not teach, disclose, or suggest first and second semiconductor dies attached to a top surface of a substrate and first and second heat spreaders attached to a bottom surface of

the substrate, where the first and second semiconductor dies are connected to the first and second heat spreaders by first and second vias, respectively. Terasawa specifically discloses semiconductor module 70, which includes element control circuits 2, which are mounted on wiring conductors 32 situated on the surface of wiring substrates 30, respectively. See, for example, column 6, lines 47-51 and Figure 1 of Terasawa. In Terasawa, element control circuits 2 are connected to shield conductors 33, which are situated inside respective wiring substrates 30. See, for example, column 6, lines 50-58 and Figure 1 of Terasawa. Thus, in Terasawa, element control circuits 2 are attached to the respective surfaces of different wiring substrates, i.e. wiring substrates 30, not a single substrate as specified by independent claim 1. Furthermore, shield conductors 33 are situated inside respective wiring substrates 30 and, as such, are not similar to heat spreaders that are situated on the bottom of a substrate. Moreover, Terasawa does not teach, disclose, or suggest a single substrate that includes heat spreaders attached to a bottom surface of the substrate coupled by respective vias to semiconductor dies attached to the top surface of the substrate.

For all the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claim 1, is not suggested, disclosed, or taught by Selna and Terasawa, either singly or in combination. Thus, independent claim 1 is patentably distinguishable over Selna and Terasawa and, as such, claims 2-13 depending from independent claim 1are, *a fortiori*, also patentably distinguishable over Selna and

Terasawa for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The present invention, as defined by independent claim 14, teaches, among other things, first and second semiconductor dies attached to a top surface of a substrate and a heat spreader attached to a bottom surface of the substrate, where the first and second semiconductor dies are connected to the heat spreader by first and second vias, respectively. The present invention, as defined by independent claim 14, provides similar electrical and thermal advantages as discussed above in relation to independent claim 1. Additionally, as disclosed in the present application, by coupling a single heat spreader on a bottom surface of a substrate to two semiconductor dies attached to a top surface of the substrate, the present invention achieves a further reduction in inductive and resistive paths and more efficient heat conduction between the semiconductor dies and the heat spreader.

In contrast to the present invention as defined by independent claim 14, Selna does not teach, disclose, or suggest first and second semiconductor dies attached to a top surface of a substrate and a heat spreader attached to a bottom surface of the substrate, where the first and second semiconductor dies are connected to the heat spreader by first and second vias, respectively. As discussed above, Selna specifically discloses BGA package 50, which includes IC die 12 attached to the upper surface of BGA package 50 and trace 10C attached to the lower surface of BGA package 50. However, Selna does not teach, disclose, or suggest attaching two semiconductor dies to a top surface of a

substrate and connecting the two dies to a single heat spreader attached to the bottom surface of the substrate by respective vias.

In contrast to the present invention as defined by independent claim 14, Terasawa does not teach, disclose, or suggest first and second semiconductor dies attached to a top surface of a substrate and a heat spreader attached to a bottom surface of the substrate, where the first and second semiconductor dies are connected to the heat spreader by first and second vias, respectively. As discussed above, Terasawa specifically discloses shield conductors 33, which are situated inside respective wiring substrates 30. However, Terasawa fails to teach a heat spreader attached to a bottom surface of a substrate, where first and second semiconductor dies, which are attached to a top surface of the substrate, are connected to the heat spreader by respective first and second vias.

For all the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claim 14, is not suggested, disclosed, or taught by Selna and Terasawa, either singly or in combination. Thus, independent claim 14 is patentably distinguishable over Selna and Terasawa and, as such, claims 15-23 depending from independent claim 14 are, *a fortiori*, also patentably distinguishable over Selna and Terasawa for at least the reasons presented above and also for additional limitations contained in each dependent claim.

C. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1 and 14 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-23 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-23 pending in the present application is respectfully requested.

Respectfully Submitted,
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